500V 13A N-Channel Enhancement Mode Power MOSFET

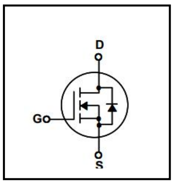
General Description

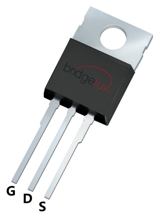
BXP13N50 is Bridgelux high voltage MOSFET family based on advanced planar DMOS technology. This advanced MOSFET family has optimized on-state resistance, and also provides superior switching performance and higher avalanche energy strength. This device family is suitable for high efficiency switch mode power supplies.

FEATURES

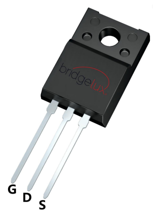
- RDSON⩽0.46Ω @Vgs=10V, Id=6.5A
- Excellent $R_{DS(ON)}$ and Low Gate Charge
- Fast switching capability
- Lead free product is acquired

SYMBOL





TO-220



TO-220F

ASSEMBLY MESSAGE

Product Name	Package	Packaging
BXP13N50P	TO-220	Tube
BXP13N50F	TO-220F	Tube

ABSOLUTE MAXIMUM RATINGS (T_C=25°C unless otherwise noted)

Parameter		Symbol	Rating		Unit
			BXP13N50P	BXP13N50F	
Drain-Source Voltage		V_{DSS}	500		V
Drain Current	Continuous (T_C = 25°C)	I_D	13		A
	Continuous (T_C = 100°C)		8.1		A
Drain Current	Pulsed (Note1)	I_{DM}	52		A
Gate-Source Voltage		V_{GSS}	±30		V
Avalanche Energy	Single Pulse (Note2)	E_{AS}	853		mJ
Avalanche Current (Note1)		I_{AR}	13		A
Peak Diode Recovery dv/dt (Note3)		dv/dt	4.5		V/ns
Power Dissipation (Note 2)	T_C =25°C	P_D	158	51	W
	Derate above 25°C		1.26	0.41	W/°C
Maximum Junction Temperature		T_J	150		°C
Storage Temperature Range		T_{STG}	-55 to 150		°C

Note：
1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. L=10.1mH, I_{AS}=13.0A, V_{DD}=50V, RG=25 Ω, Starting TJ = 25°C
3. I_{SD} ≤ 13.0A, di/dt ≤ 300A/μs, V_{DD} ≤ BV_{DSS}, Starting TJ = 25°C

THERMAL CHARACTERISTICS

Parameter	Symbol	Max.		Unit
		BXP13N50P	BXP13N50F	
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	0.79	2.45	°C / W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	62.5	62.5	°C / W

ELECTRICAL CHARACTERISTICS （T_J=25℃,unless otherwise Noted）

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	VGS=0V, ID=250μA	500			V
Zero Gate Voltage Drain Current	I_{DSS}	VDS=500V, VGS=0V			1	uA
		VDS=400V, TC = 125°C			100	uA
Gate-Body Leakage Current, Forward	I_{GSS}	VGS=30V			100	nA
Gate-Body Leakage Current, Reverse		VGS=-30V			-100	nA
Breakdown Voltage Temperature Coefficient	△BVDSS/△TJ	ID = 250 μA		0.5		V/℃
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(TH)}$	VDS=VGS, ID=250μA	2		4	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	VGS=10V, ID=6.5A		0.38	0.46	Ω
Forward Transconductance (Note4)	g_{FS}	VDS = 50V, ID=6.5A		16		S
DYNAMIC PARAMETERS						
Input Capacitance	C_{ISS}	VDS=25V, VGS=0V, f=1.0MHz		1530		pF
Output Capacitance	C_{OSS}			200		pF
Reverse Transfer Capacitance	C_{RSS}			26		pF
SWITCHING PARAMETERS						
Turn-ON Delay Time	$t_{D(ON)}$	VDD=250V, ID=13A, VGS = 10V ,RG=10Ω (Note4,5)		88		ns
Turn-ON Rise Time	t_R			150		ns
Turn-OFF Delay Time	$t_{D(OFF)}$			139		ns
Turn-OFF Fall-Time	t_F			55		ns
Total Gate Charge(Note5)	Q_G	VDS =400V, VGS =10V, ID =13A (Note4,5)		38		nC
Gate Source Charge	Q_{GS}			10.5		nC
Gate Drain Charge	Q_{GD}			16.8		nC
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS						
Drain-Source Diode Forward Voltage	V_{SD}	IS=6.5A, VGS=0V			1.4	V
Diode Continuous Forward Current	I_S				13	A
Pulsed Drain-Source Current	I_{SM}				52	A
Reverse Recovery Time	t_{RR}	VGS = 0 V, ISD = 13A di/dt=100 A/μs (Note4,5)		405		ns
Reverse Recovery Charge	Q_{RR}			4.6		uC

Note： 4. Pulse Test : Pulse width ≤ 300μs, Duty cycle ≤ 2%
5. Essentially independent of operating temperature

TYPICAL CHARACTERISTICS

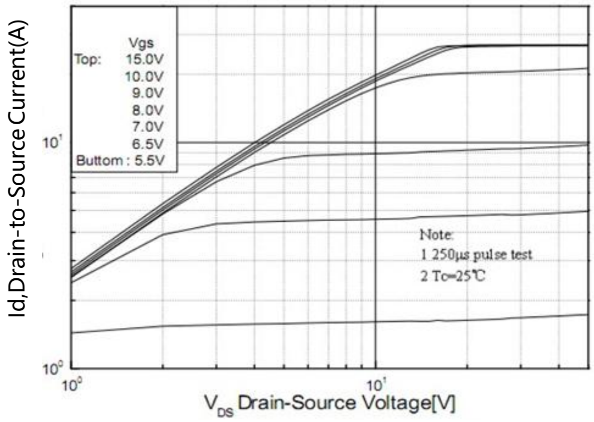


Figure1. Typical Output Characteristics

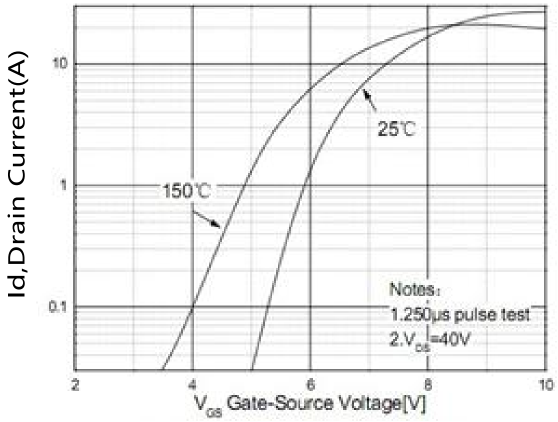


Figure2. Typical Transfer Characteristics

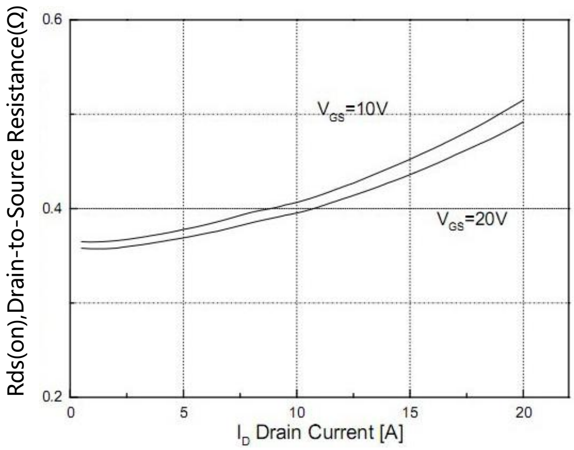


Figure3. On-Resistance versus Drain Current

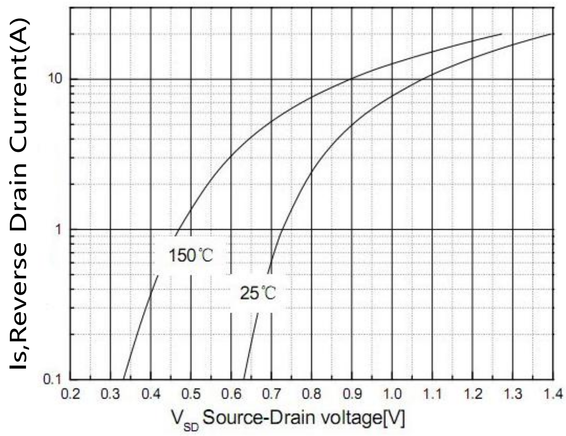


Figure4. Diode forward voltage versus Current

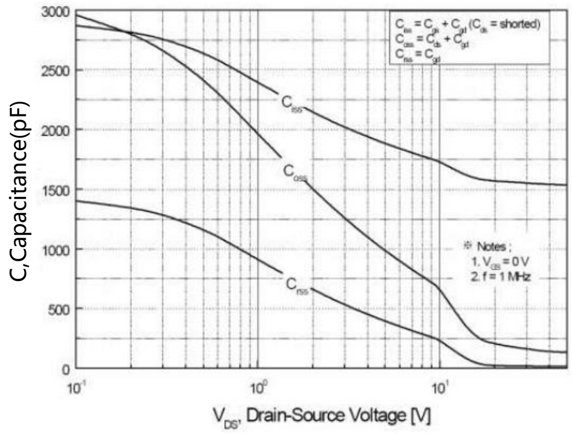


Figure5. Typical Capacitance versus V_{DS}

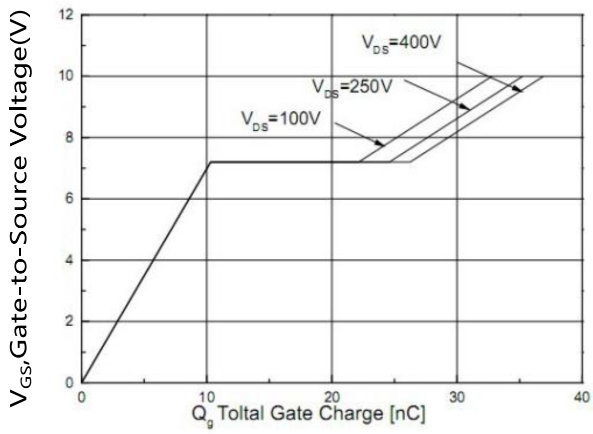


Figure6. Typical Gate Charge versus V_{GS}

TYPICAL CHARACTERISTICS(Cont.)

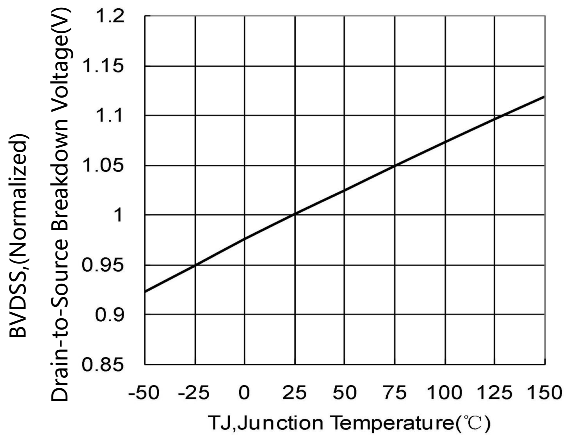


Figure7. BV_{DSS} Variation with Temperature

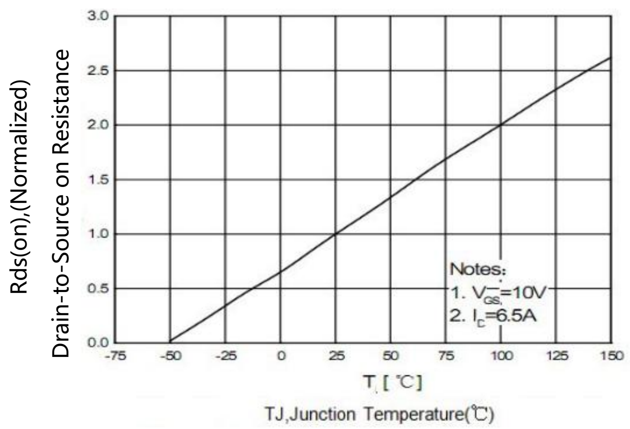


Figure8. On-Resistance Variation with Temperature

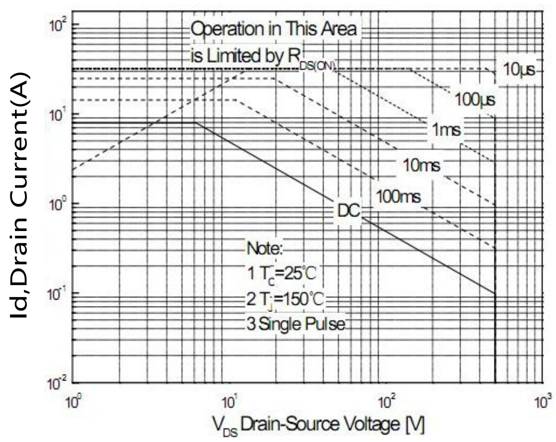


Figure9. Maximum Safe Operating Area

BXP13N50P

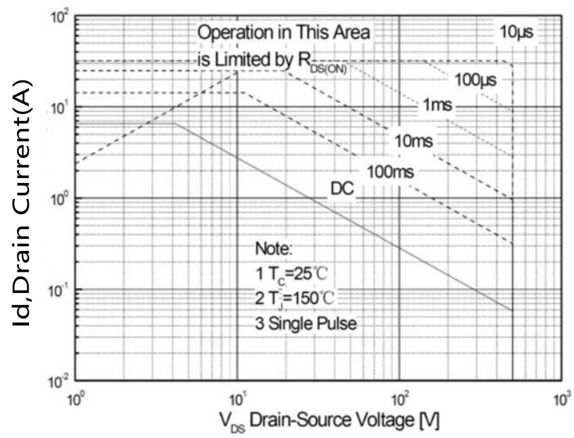


Figure9. Maximum Safe Operating Area

BXP13N50F

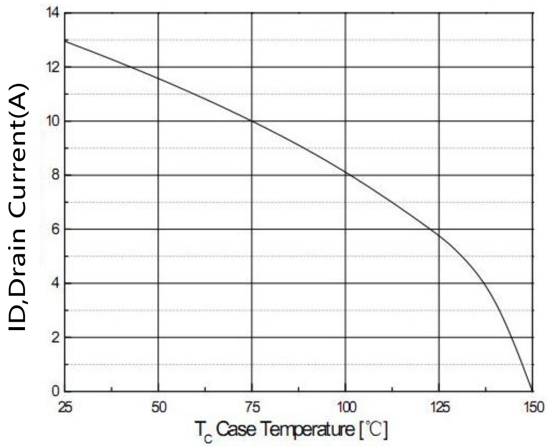
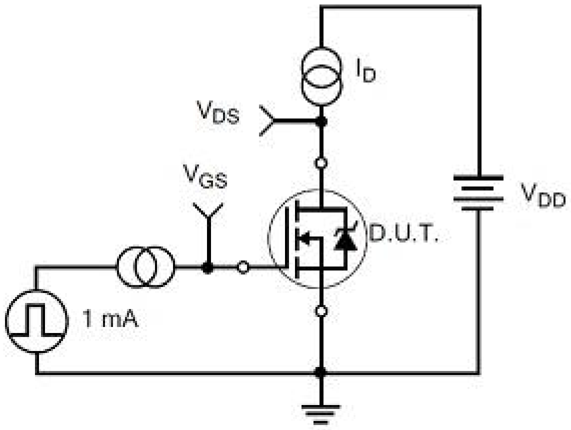


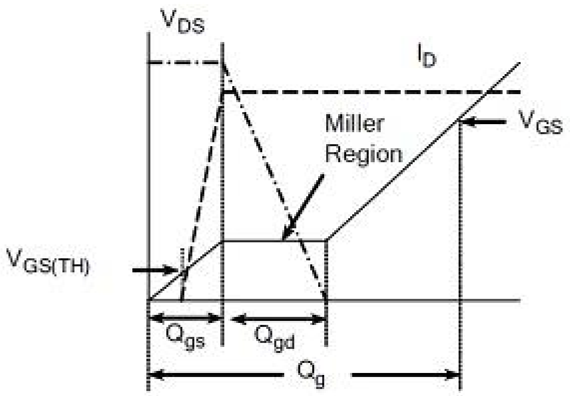
Figure10. Maximum Continuous Drain Current

versus Case Temperature

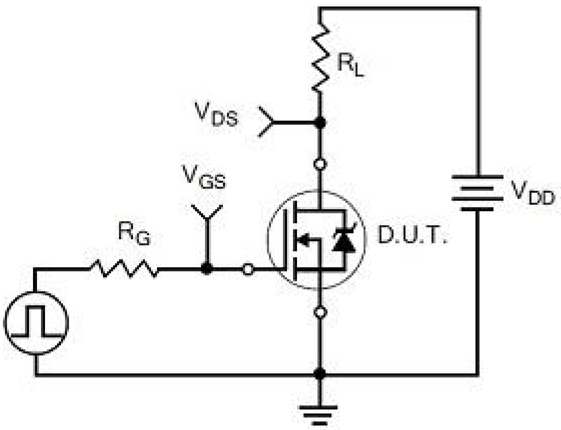
TEST CIRCUITS AND WAVEFORMS



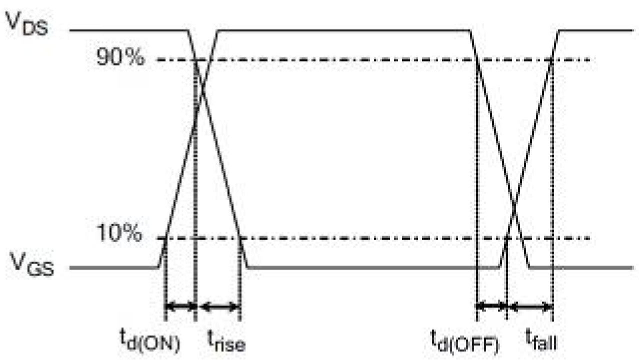
Gate Charge Test Circuit



Gate Charge Waveform

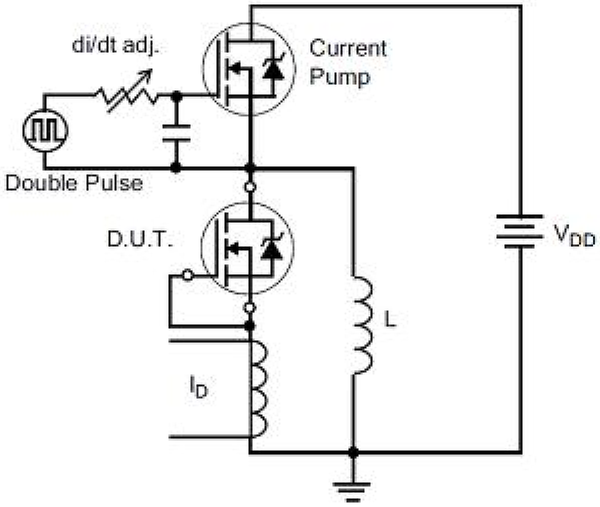


Resistive Switching Test Circuit

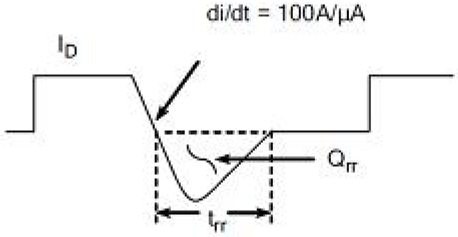


Resistive Switching Waveforms

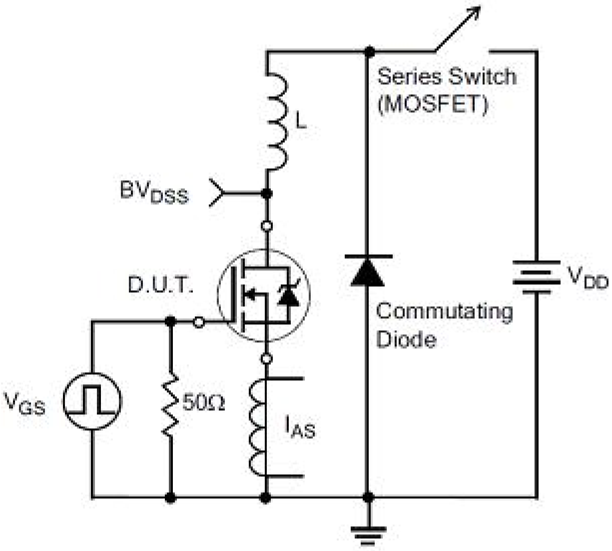
TEST CIRCUITS AND WAVEFORMS(Cont.)



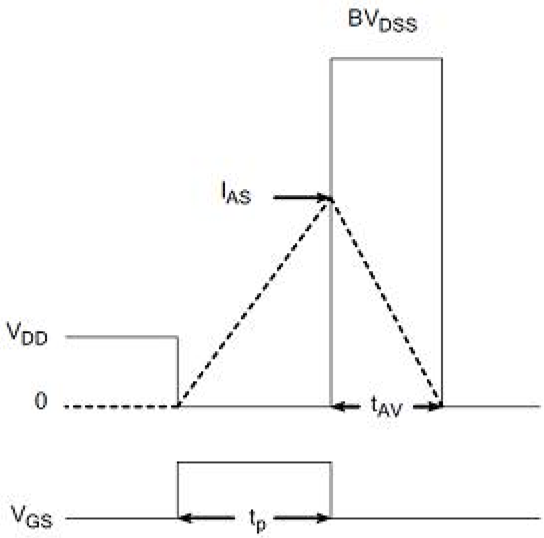
Diode Reverse Recovery Test Circuit



Diode Reverse Recovery Waveform



Unclamped Inductive Switching Test Circuit



$$E_{AS} = \frac{I_{AS}^2 L}{2}$$

Unclamped Inductive Switching Waveforms

Revision history

Document revision history

Date	Revision	Changes
15-Mar-2021	1.0	First release
6-Jan-2022	1.1	Update parameter

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